HT1625

RAM Mapping 64×8 LCD Controller for I/O MCU

PATENTED

PAT No. : 099352

Technical Document

- Application Note

Features

- Operating voltage: 2.7V~5.2V
- Built-in RC oscillator
- External 32.768kHz crystal or 32kHz frequency source input
- 1/4 bias, 1/8 duty, frame frequency is 64Hz
- Max. 64×8 patterns, 8 commons, 64 segments
- Built-in internal resistor type bias generator
- 3-wire serial interface
- 8 kinds of time base or WDT selection
- Time base or WDT overflow output
- Built-in LCD display RAM
- R/W address auto increment
- Two selectable buzzer frequencies (2kHz or 4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- VLCD pin to adjust LCD operating voltage
- 100-pin QFP package

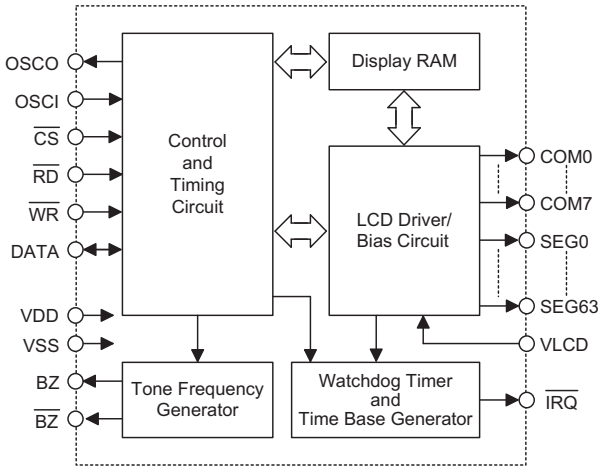
General Description

HT1625 is a peripheral device specially designed for I/O type MCU used to expand the display capability. The max. display segment of the device are 512 patterns (64×8). It also supports serial interface, buzzer sound, Watchdog Timer or time base timer functions. The HT1625 is a memory mapping and multi-function LCD controller. The software configuration feature of the HT1625 make it suitable for multiple LCD applications including LCD modules and display subsystems. Only three lines are required for the interface between the host controller and the HT1625. The HT162X series have many kinds of products that match various applications.

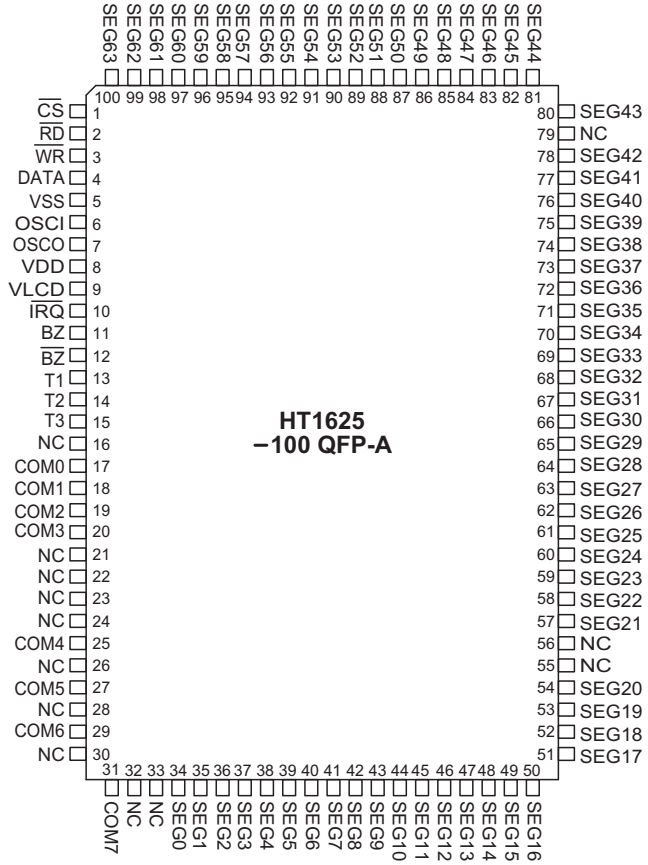
Selection Table

HT162X	HT1620	HT1621	HT1622	HT16220	HT1623	HT1625	HT1626
COM	4	4	8	8	8	**8**	16
SEG	32	32	32	32	48	**64**	48
Built-in Osc.	—	√	√	—	√	√	√
Crystal Osc.	√	√	—	√	√	√	√

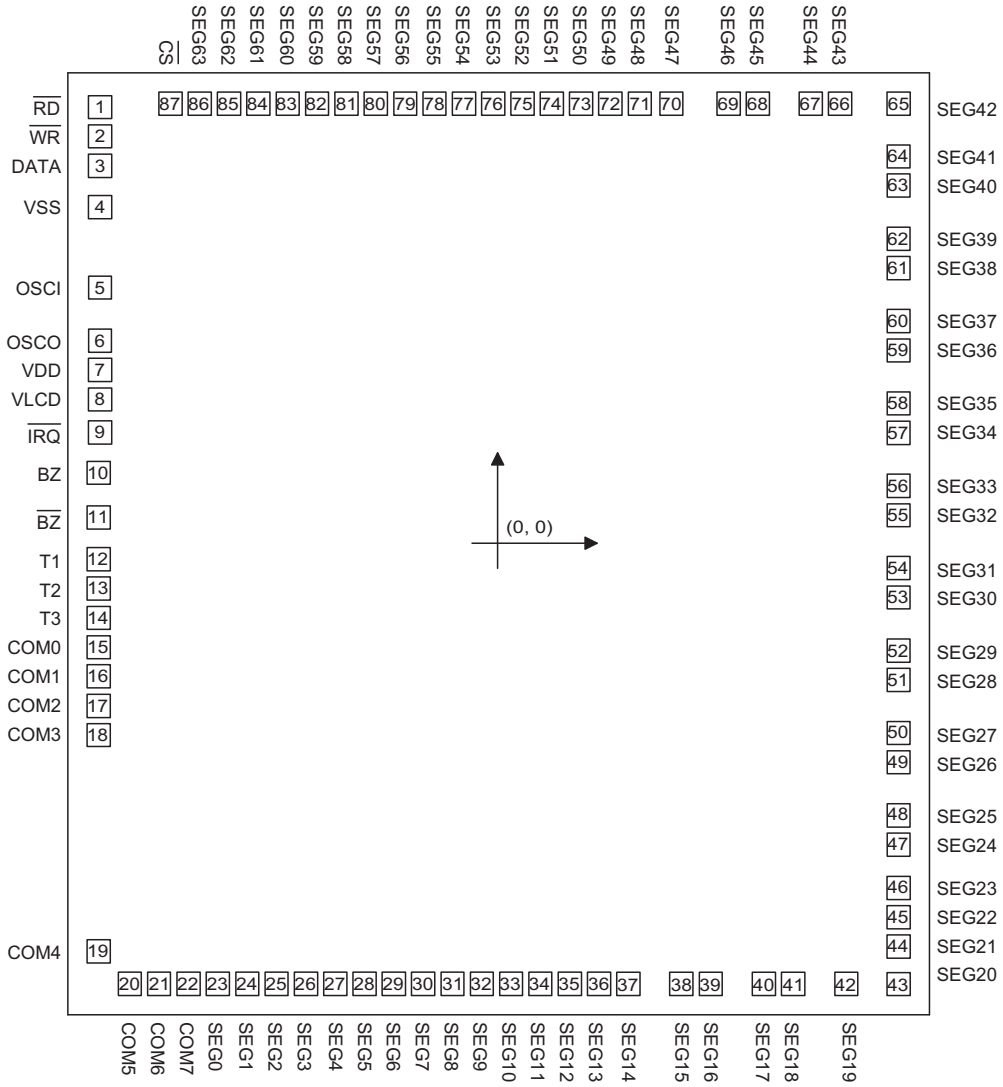
Block Diagram



Pin Assignment



Pad Assignment



Chip size: 118 × 128 (mil)^2

* The IC substrate should be connected to VDD in the PCB layout artwork.

Pad Coordinates

Unit: μm

Pad No.	X	Y	Pad No.	X	Y
1	–1399.087	1514.994	45	1396.978	–1327.281
2	–1399.087	1415.973	46	1396.978	–1228.182
3	–1399.087	1316.263	47	1396.978	–1082.807
4	–1399.087	1140.800	48	1396.978	–983.707
5	–1399.087	876.062	49	1396.978	–798.327
6	–1399.087	684.333	50	1396.978	–699.227
7	–1399.087	585.273	51	1396.978	–513.846
8	–1399.087	486.214	52	1396.978	–414.747
9	–1399.087	387.114	53	1396.978	–229.367
10	–1400.132	237.773	54	1396.978	–130.266
11	–1400.132	87.535	55	1396.978	55.114
12	–1400.132	–53.536	56	1396.978	154.214
13	–1400.132	–152.637	57	1396.978	339.594
14	–1400.132	–251.656	58	1396.978	438.693
15	–1400.132	–350.758	59	1396.978	624.073
16	–1400.132	–449.776	60	1396.978	723.173
17	–1400.132	–548.878	61	1396.978	908.553
18	–1400.132	–647.896	62	1396.978	1007.654
19	–1400.132	–1401.530	63	1396.978	1193.033
20	–1254.633	–1523.957	64	1396.978	1292.134
21	–1155.531	–1523.957	65	1364.057	1521.618
22	–1056.513	–1523.957	66	1172.328	1521.618
23	–957.411	–1523.957	67	1073.228	1521.618
24	–858.392	–1523.957	68	881.497	1521.618
25	–759.292	–1523.957	69	782.397	1521.618
26	–660.272	–1523.957	70	590.667	1521.618
27	–561.172	–1523.957	71	485.994	1521.618
28	–462.153	–1523.957	72	386.972	1521.618
29	–363.052	–1523.957	73	287.874	1521.618
30	–264.033	–1523.957	74	188.852	1521.618
31	–164.932	–1523.957	75	89.753	1521.618
32	–65.912	–1523.957	76	–9.267	1521.618
33	33.188	–1523.957	77	–108.367	1521.618
34	132.208	–1523.957	78	–207.387	1521.618
35	231.309	–1523.957	79	–306.487	1521.618
36	330.328	–1523.957	80	–405.508	1521.618
37	429.159	–1523.957	81	–504.607	1521.618
38	614.539	–1523.957	82	–603.628	1521.618
39	713.638	–1523.957	83	–702.727	1521.618
40	899.018	–1523.957	84	–801.747	1521.618
41	998.119	–1523.957	85	–900.846	1521.618
42	1183.499	–1523.957	86	–999.868	1521.618
43	1396.978	–1525.401	87	–1098.967	1521.618
44	1396.978	–1426.302			

Pad Description

Pad No.	Pad Name	I/O	Description
1	$\overline{RD}$	I	READ clock input with pull-high resistor. Data in the RAM of the HT1625 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the data line. The host controller can use the next rising edge to latch the clocked out data.
2	$\overline{WR}$	I	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the HT1625 on the rising edge of the $\overline{WR}$ signal.
3	DATA	I/O	Serial data input or output with pull-high resistor
4	VSS	—	Negative power supply, ground
5	OSCI	I	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
6	OSCO	O	
7	VDD	—	Positive power supply
8	VLCD	I	LCD operating voltage input pad.
9	$\overline{IRQ}$	O	Time base or Watchdog Timer overflow flag, NMOS open drain output
10, 11	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair
12~14	T1~T3	I	Not connected
15~22	COM0~COM7	O	LCD common outputs
23~86	SEG0~SEG63	O	LCD segment outputs
87	$\overline{CS}$	I	Chip selection input with pull-high resistor. When the $\overline{CS}$ is logic high, the data and command read from or write to the HT1625 are disabled. The serial interface circuit is also reset. But if the $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the HT1625 are all enabled.

Absolute Maximum Ratings

Supply Voltage .....–0.3V to 5.5V

Input Voltage.....V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature .....–50°C to 125°C

Operating Temperature.....–25°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.7	—	5.2	V
I_{DD1}	Operating Current	3V	No load or LCD ON On-chip RC oscillator	—	155	310	μA
		5V		—	260	420	μA
I_{DD2}	Operating Current	3V	No load or LCD ON Crystal oscillator	—	150	310	μA
		5V		—	250	420	μA
I_{DD11}	Operating Current	3V	No load or LCD OFF On-chip RC oscillator	—	8	30	μA
		5V		—	20	60	μA
I_{DD22}	Operating Current	3V	No load or LCD OFF Crystal oscillator	—	—	20	μA
		5V		—	—	35	μA
I_{STB}	Standby Current	3V	No load, Power down mode	—	1	12	μA
		5V		—	2	24	μA
V_{IL}	Input Low Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V_{IH}	Input High Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	—	3	V
		5V		4.0	—	5	V
I_{OL1}	BZ, $\overline{BZ}$, $\overline{IRQ}$	3V	V_{OL}=0.3V	0.9	1.8	—	mA
		5V	V_{OL}=0.5V	1.7	3	—	mA
I_{OH1}	BZ, $\overline{BZ}$	3V	V_{OH}=2.7V	–0.9	–1.8	—	mA
		5V	V_{OH}=4.5V	–1.7	–3	—	mA
I_{OL1}	DATA	3V	V_{OL}=0.3V	0.9	1.8	—	mA
		5V	V_{OL}=0.5V	1.7	3	—	mA
I_{OH1}	DATA	3V	V_{OH}=2.7V	–0.9	–1.8	—	mA
		5V	V_{OH}=4.5V	–1.7	–3	—	mA
I_{OL2}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	160	—	μA
		5V	V_{OL}=0.5V	180	360	—	μA
I_{OH2}	LCD Common Source Current	3V	V_{OH}=2.7V	–40	–80	—	μA
		5V	V_{OH}=4.5V	–90	–180	—	μA
I_{OL3}	LCD Segment Sink Current	3V	V_{OL}=0.3V	50	100	—	μA
		5V	V_{OL}=0.5V	120	240	—	μA
I_{OH3}	LCD Segment Source Current	3V	V_{OH}=2.7V	–30	–60	—	μA
		5V	V_{OH}=4.5V	–70	–140	—	μA
R_{PH}	Pull-high Resistor	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	100	200	300	kΩ
		5V		50	100	150	kΩ

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System Clock	5V	On-chip RC oscillator	24	32	40	kHz
f_{SYS2}	System Clock	—	External clock source	—	32	—	kHz
f_{LCD1}	LCD Frame Frequency	5V	On-chip RC oscillator	48	64	80	Hz
f_{LCD2}	LCD Frame Frequency	—	External clock source	—	64	—	Hz

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{COM}	LCD Common Period	—	n: Number of COM	—	n/f_{LCD}	—	sec
f_{CLK1}	Serial Data Clock ($\overline{WR}$ Pin)	3V	Duty cycle 50%	4	—	150	kHz
		5V		4	—	300	kHz
f_{CLK2}	Serial Data Clock ($\overline{RD}$ Pin)	3V	Duty cycle 50%	—	—	75	kHz
		5V		—	—	150	kHz
t_{CS}	Serial Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	700	800	—	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	125	μs
			Read mode	6.67	—	—	
		5V	Write mode	1.67	—	125	μs
			Read mode	3.34	—	—	
t_r, t_f	Rise or Fall Time Serial Data Clock Width (Figure 1)	—	—	—	120	160	ns
tsu	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	—	—	60	120	—	ns
t_h	Hold Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	—	—	700	800	—	ns
t_{su1}	Setup Time for CS to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	—	—	500	600	—	ns
t_{h1}	Hold Time for CS to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	—	—	50	100	—	ns
f_{tone}	Tone Frequency (2KHz)	5V	On-chip RC oscillator	1.5	2.0	2.5	kHz
	Tone Frequency (4KHz)			3.0	4.0	5.0	kHz
t_{OFF}	V_{DD} OFF Times (Figure 4)	—	VDD drop down to 0V	20	—	—	ms
t_{SR}	V_{DD} Rising Slew Rate (Figure 4)	—	—	0.05	—	—	V/ms

Note: 1. If the conditions of Power-on Reset timing are not satisfied in power On/Off sequence, the internal Power-on Reset (POR) circuit will not operate normally.
2. If the VDD drops below the minimum voltage of operating voltage spec. during operating, the conditions of Power-on Reset timing must be satisfied also. That is, the VDD must drop to 0V and keep at 0V for 20ms (min.) before rising to the normal operating voltage.

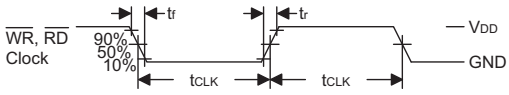


Figure 1

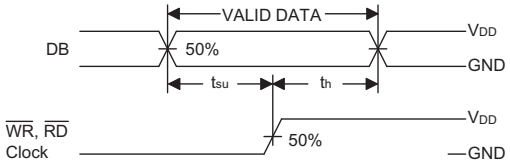


Figure 2

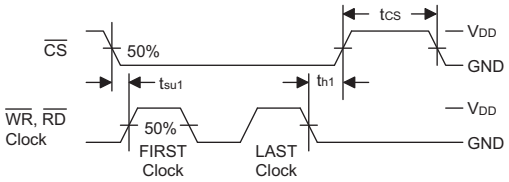


Figure 3

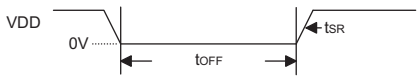


Figure 4 Power-on Reset Timing

Functional Description

Display memory – RAM structure

The static display RAM is organized into 128×4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

Time base and Watchdog Timer – WDT

The time base generator and WDT share the same divided (/256) counter. TIMER DIS/EN/CLR
, WDT DIS/EN/CLR and $\overline{IRQ}$ EN/DIS are independent from each other. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will remain at logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued.

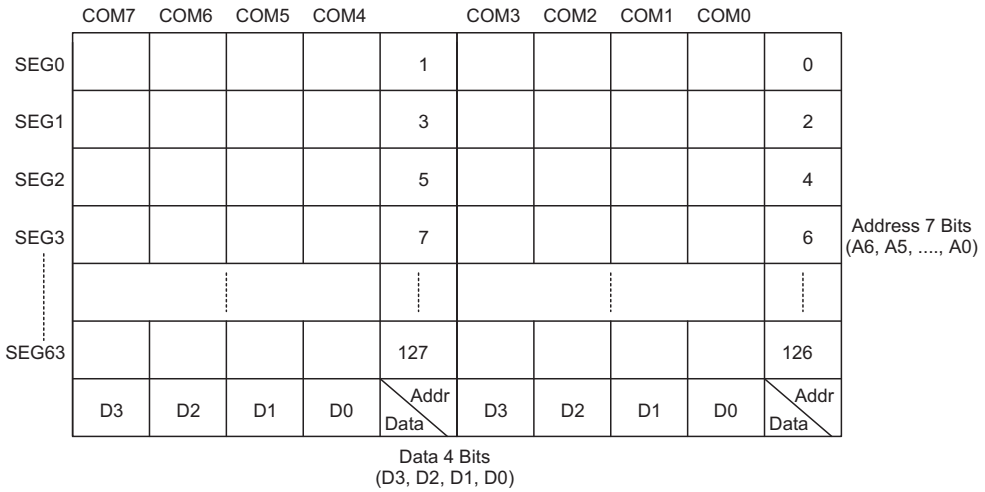
If an external clock is selected as the source of system frequency, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.

Buzzer tone output

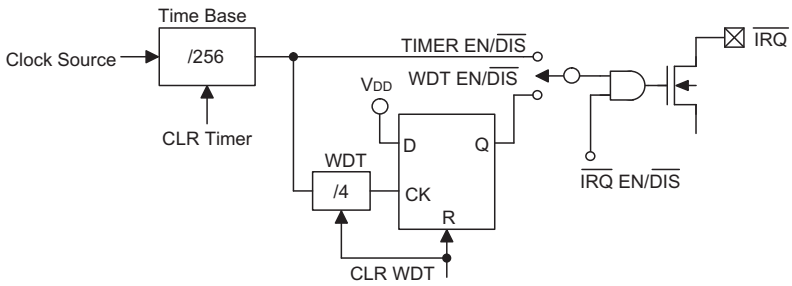
A simple tone generator is implemented in the HT1625. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$ which are used to generate a single tone.

Command format

The HT1625 can be configured by the software setting. There are two mode commands to configure the HT1625 resource and to transfer the LCD display data.



RAM mapping



Timer and WDT configurations

The following are the data mode ID and the command mode ID:

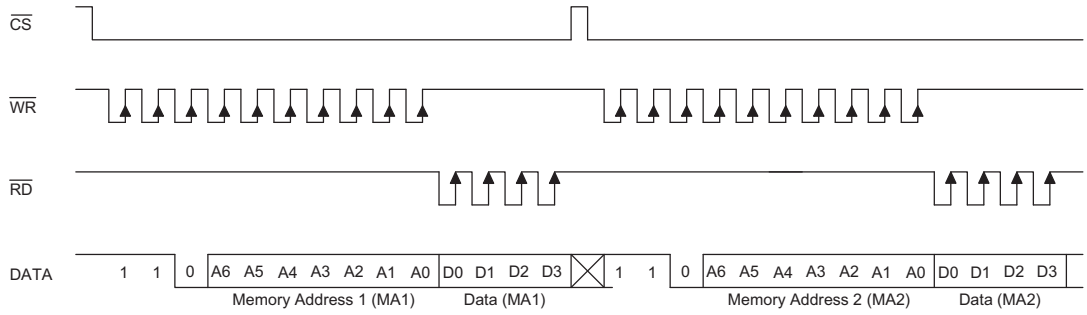
Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will be reset also. The $\overline{CS}$ pin returns to "0", a new operation mode ID should be issued first.

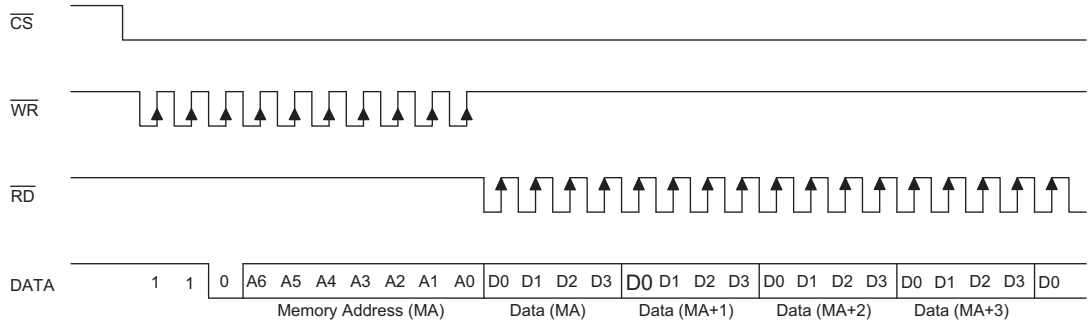
Name	Command Code	Function
TONE OFF	0000-1000-X	Turn-off tone output
TONE 4K	010X-XXXX-X	Turn-on tone output, tone frequency is 4kHz
TONE 2K	0110-XXXX-X	Turn-on tone output, tone frequency is 2kHz

Timing Diagrams

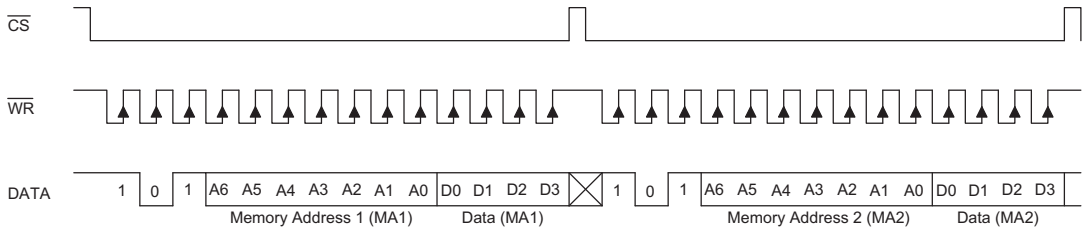
READ mode (command code : 1 1 0)



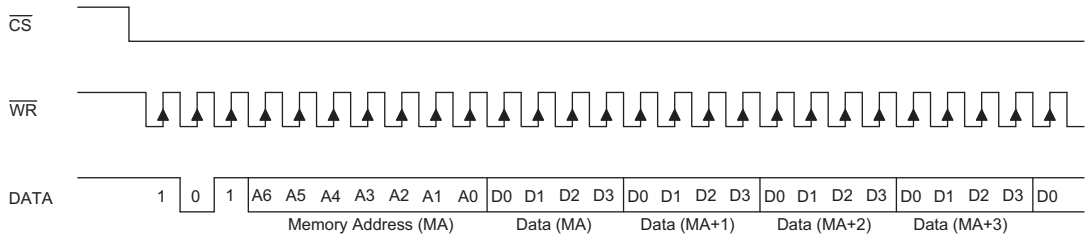
READ mode (successive address reading)



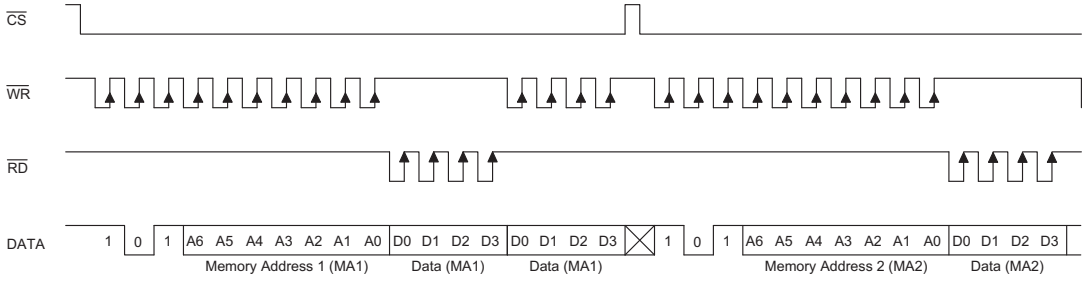
WRITE mode (command code : 1 0 1)



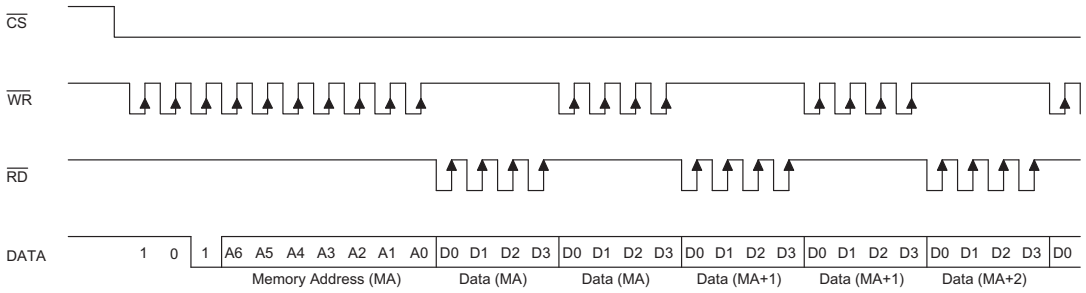
WRITE mode (successive address writing)



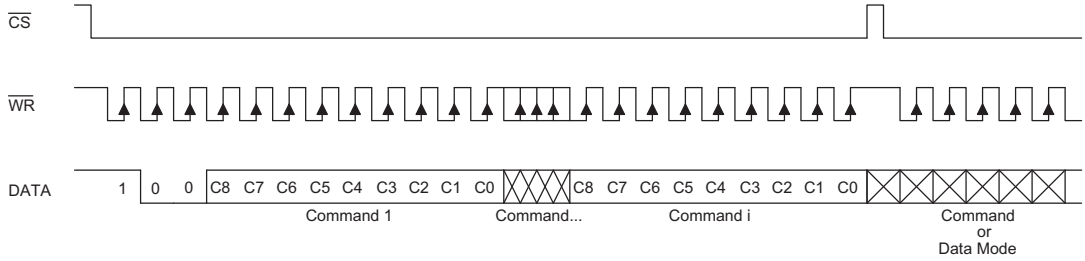
READ-MODIFY-WRITE mode (command code : 1 0 1)



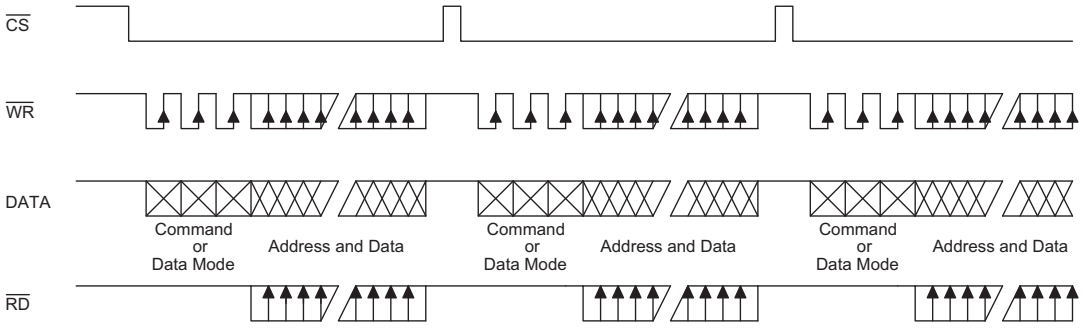
READ-MODIFY-WRITE mode (successive address accessing)



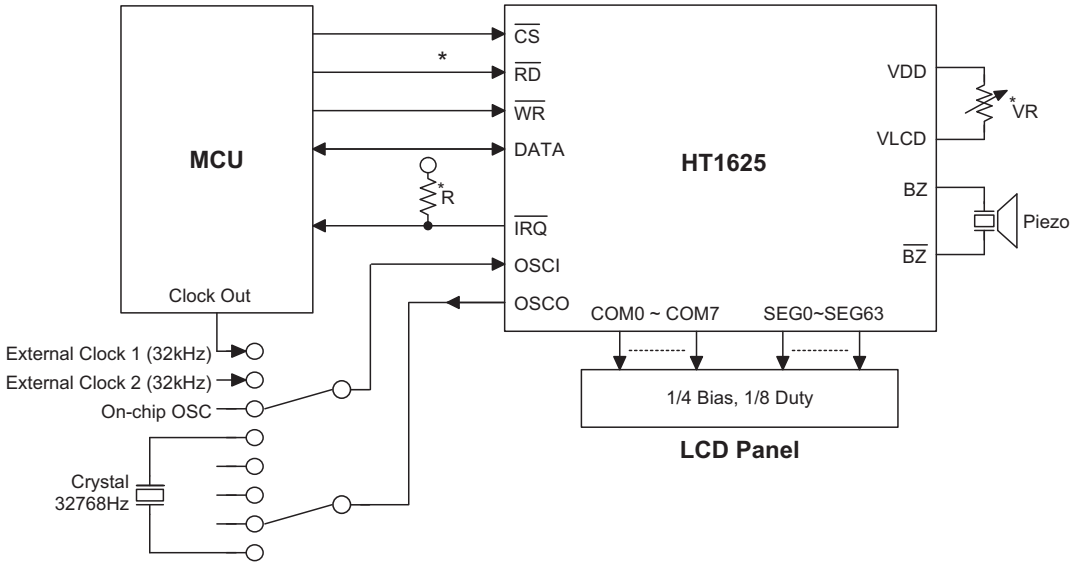
Command mode (command code : 1 0 0)



Mode (data and command mode)



Application Circuits



Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the requirement of the MCU.

The voltage applied to V_{LCD} pin must be lower than V_{DD}.

Adjust VR to fit LCD display, at V_{DD}=5V, V_{LCD}=4V, VR=15kΩ±20%.

Adjust R (external Pull-high resistance) to fit user's time base clock.

Instruction Set Summary

Name	ID	Command Code	D/C	Function	Def.
READ	**1 1 0**	A6A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	**1 0 1**	A6A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	**1 0 1**	A6A5A4A3A2A1A0D0D1D2D3	D	Read and Write data to the RAM	
SYS DIS	**1 0 0**	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	**1 0 0**	0000-0001-X	C	Turn on system oscillator	
LCD OFF	**1 0 0**	0000-0010-X	C	Turn off LCD display	Yes
LCD ON	**1 0 0**	0000-0011-X	C	Turn on LCD display	
TIMER DIS	**1 0 0**	0000-0100-X	C	Disable time base output	Yes
WDT DIS	**1 0 0**	0000-0101-X	C	Disable WDT time-out flag output	Yes
TIMER EN	**1 0 0**	0000-0110-X	C	Enable time base output	
WDT EN	**1 0 0**	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	**1 0 0**	0000-1000-X	C	Turn off tone outputs	Yes
CLR TIMER	**1 0 0**	0000-1101-X	C	Clear the contents of the time base generator	
CLR WDT	**1 0 0**	0000-1111-X	C	Clear the contents of the WDT stage	
RC 32K	**1 0 0**	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes
EXT (XTAL) 32K	**1 0 0**	0001-11XX-X	C	System clock source, external 32kHz clock source or crystal oscillator 32.768kHz	

Name	ID	Command Code	D/C	Function	Def.
TONE 4K	**1 0 0**	010X-XXXX-X	C	Tone frequency output: 4kHz	
TONE 2K	**1 0 0**	0110-XXXX-X	C	Tone frequency output: 2kHz	
$\overline{\text{IRQ}}$ DIS	**1 0 0**	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	Yes
$\overline{\text{IRQ}}$ EN	**1 0 0**	100X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	
F1	**1 0 0**	101X-0000-X	C	Time base clock output: 1Hz The WDT time-out flag after: 4s	
F2	**1 0 0**	101X-0001-X	C	Time base clock output: 2Hz The WDT time-out flag after: 2s	
F4	**1 0 0**	101X-0010-X	C	Time base clock output: 4Hz The WDT time-out flag after: 1s	
F8	**1 0 0**	101X-0011-X	C	Time base clock output: 8Hz The WDT time-out flag after: 1/2s	
F16	**1 0 0**	101X-0100-X	C	Time base clock output: 16Hz The WDT time-out flag after: 1/4s	
F32	**1 0 0**	101X-0101-X	C	Time base clock output: 32Hz The WDT time-out flag after: 1/8s	
F64	**1 0 0**	101X-0110-X	C	Time base clock output: 64Hz The WDT time-out flag after: 1/16s	
F128	**1 0 0**	101X-0111-X	C	Time base clock output: 128Hz The WDT time-out flag after: 1/32s	Yes
TEST	**1 0 0**	1110-0000-X	C	Test mode, user don't use.	
NORMAL	**1 0 0**	1110-0011-X	C	Normal mode	Yes

Note: X : Don't care

A6~A0 : RAM address

D3~D0 : RAM data

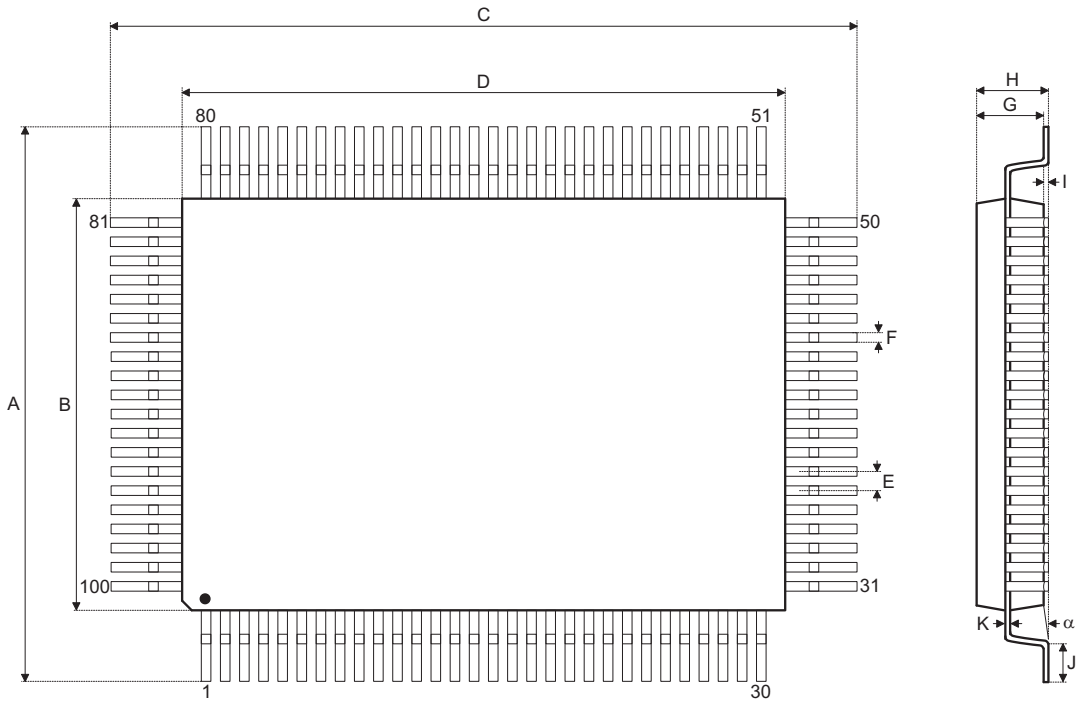
D/C : Data/Command mode

Def. : Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base or WDT clock frequency can be derived from an on-chip 32kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1625 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the HT1625.

Package Information

100-pin QFP (14mm×20mm) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	18.50	—	19.20
B	13.90	—	14.10
C	24.50	—	25.20
D	19.90	—	20.10
E	—	0.65	—
F	—	0.30	—
G	2.50	—	3.10
H	—	—	3.40
I	—	0.10	—
J	1	—	1.40
K	0.10	—	0.20
α	0°	—	7°

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